REMARKS

Claim 61 has been amended and claims 66-69 have been added. Claims 51, 52 and 54-69 remain in the application. This Preliminary Amendment accompanies a request for Continued Prosecution Application. Examination of the claims in this preliminary amendment is requested.

Claim 61 has been amended to correct minor informalities noted during review, however, these amendments do not alter the scope of the claims.

Claims 51, 52 and 54-65 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koh et al., U.S. Patent No. 5,686,337; or Chan, U.S. Patent No. 5,627,094; or Rosner, U.S. Patent No. 5,496,757; or Kim, U.S. Patent No. 5,403,767, all previously cited, or Summerfelt, U.S. Patent No. 5,619,393.

Claim 51 recites "etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", which is not taught or disclosed by any of the cited references.

Claim 57 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 60 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first

dielectric layer; forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 61 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer; conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave partitions after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 62 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

The Examiner's rejection based on the teachings of the teachings of Koh et al. demonstrates on its face that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claims 51 and 60-62. The

Examiner indicates that the etching steps are shown in Figs. 3 and 5, while the insulative partitions are shown in Fig. 7, corresponding to a processing step subsequent to both of the etching steps.

To clarify this further, forming of a partition subsequent to two etching steps, as shown by Koh et al., is not equivalent to "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as positively recited in claim 51. In other words, Koh et al. do not teach, disclose, suggest or motivate "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", and the Examiner fails to show any such step in Koh et al.

In fact, the Examiner's *Conclusion* reiterates that Koh et al. do not teach or disclose the invention as recited in claim 51. The Examiner states (p. 4) that "Koh et al. clearly teaches an insulating layer formed between two capacitors after second etching. Applicant fails to specifically pointing [sic] out disagreements with the examiner's contentions."

Applicant specifically points out for the Examiner's benefit that teaching that something occurs after two etching steps does not teach something that occurs intermediate two etching steps. The word "intermediate" means "between", and does not mean or include "after".

To clarify this point yet further, a copy of p. 611 of the Merriam Webster's Collegiate Dictionary, 10TH Ed. (Merriam Webster, Springfield MA, copyright 1993, is enclosed. This page includes a definition of intermediate, viz., "beginning or occurring at the middle place, stage, or degree or between extremes". As such, it is abundantly clear that Koh et al. do not teach,

disclose, suggest or motivate the invention as recited in claim 51. For at least these reasons, the rejection of claim 51 based on the teachings of Koh et al. is defective and should be withdrawn, and claim 51 should be allowed.

Claim 57 recites plural anisotropic etching steps. Koh et al. teach a first embodiment with respect to Figs. 2 and 5 using (col. 5, lines 36-40) one isotropic etching step, followed by one anisotropic etch of the same structure. Koh et al. not only fail to teach plural anisotropic etching steps, Koh et al. also do not teach etching of first and then second capacitor container openings, as recited in claim 57.

To clarify these concepts, Applicants are providing copies of pages 46 and 622 of Merriam Webster's Collegiate Dictionary, 10^{TH} Ed. (Merriam Webster, Springfield MA, copyright 1993. The definition of "anisotropic" is "exhibiting properties with different values when measured in different directions". An anisotropic etch is an etch having a higher etch rate in one direction than in another.

The definition of "isotropic" is "exhibiting properties (as the velocity of light transmission) with the same values when measured along exes in all directions". An isotropic etch is an etch exhibiting the same etch rate in all directions (see, e.g., the dashed line in Fig. 3 of the Koh et al. reference).

Koh et al. teach a second embodiment with respect to Fig. 3 (see col. 6, line 4 et seq.). The second embodiment also fails to teach etching of first and then second capacitor container openings, as recited in claim 57. Koh et al. also do not teach first and second anisotropic etching steps with respect to the second embodiment. For at least these reasons, the rejection of claim

57 based on the teachings of Koh et al. is clearly defective and should be withdrawn, and claim 57 should be allowed.

Similarly, claims 60-62 provide an explicit ordering of etching, forming partitions and only then, following formation of the partitions, second etching. Again, the Examiner's own conclusion shows clearly that Koh et al. cannot possibly provide the invention as recited in these claims. Koh et al. teach formation of the partitions after both of the etching steps. For at least these reasons, the rejection of claims 60-62 based on the teachings of Koh et al. are clearly defective and should be withdrawn, and claims 60-62 should be allowed.

Chan et al. teach formation of a patterned planarized first dielectric layer 20b in a first anisotropic etching step (Fig. 2b; col. 8, lines 25-35). This step also defines capacitor container openings. As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51 and 60-62.

More specifically, Chan et al. teach formation of an insulator 20 (Fig. 2a). A patterned mask layer 24b is then formed (Fig. 2b; col. 7, lines 11-17). The insulator 20 is then etched to form dielectric layer portion 20b (Fig. 2b). The patterned portion 22b of the second dielectric layer is then completely etched (Fig. 2c and col. 8, line 57 through col. 9, line 6).

Because the dielectric layer portion 20b is formed during the first etching step and thus is shown clearly in Fig. 2b, it cannot be the result of "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as recited in claim 51.

Claim 57 recites first and second anisotropic etching steps. The second etching step taught by Chan et al. is an isotropic etching step (col. 8, lines 61 and 62). The undercutting needed to remove the portion 24b cannot be carried out using anisotropic etching. Similarly, claims 60-62 provide an explicit ordering of anisotropic etching, forming partitions and only then, following formation of the partitions, second anisotropic etching.

Attempting to adapt the teachings of Chan et al. to arrive at the subject matter recited in claims 57 and 60-62 defeats the main intent of Chan et al. and also makes the teachings of Chan et al. unsuitable for their intended purposes. It is improper to modify the teachings of a reference in such a manner (see MPEP §§ 2145(X), 2141.02 and 2143.01).

As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51, 57 and 60-62. For at least these reasons, the rejections of claims 51, 57 and 60-62 based on the teachings of Chan et al. are defective and should be withdrawn, and claims 51, 57 and 60-62 should be allowed.

The Examiner's rejection based on the teachings of Rosner demonstrates on its face that Rosner does not teach, disclose, suggest or motivate the invention as recited in claim 51. The Examiner indicates that the etching steps are shown in Figs. 4 and 5, while formation of the insulative partition is shown in Fig. 6, corresponding to a processing step subsequent to the etching steps. Rosner does not teach or disclose formation of an insulative partition intermediate two etching steps, as recited in claim 51.

Additionally, Rosner teaches (col. 5, lines 54 and 55) that "The first auxiliary layer 4 is then removed by wet-chemical etching using, for example, choline." Wet etching of polysilicon layer 4 (col. 5, line 17) is, by definition, isotropic etching. As a result, Rosner does not and cannot teach, disclose, suggest or motivate the invention as recited in claims 57 and 60-62.

For at least these reasons, the rejection of claims 51, 57 and 60-62 based on the teachings of the Rosner reference is defective and should be withdrawn, and claims 51, 57 and 60-62 should be allowed.

Kim '767 teaches etching first openings in an insulating layer 7 in Fig. 1C. The first openings are not capacitor container openings. Kim '767 then teaches formation of "second insulating film spacers 8A" followed by formation of "etching barrier layer 9" (Fig. 1D; col. 2, lines 42-57). Kim '767 teaches formation of capacitor containers in Fig. 1E by removal of the reminder of the insulating layer 7A, i.e., in a single etching step. As a result, Kim '767 does not and cannot teach, disclose, suggest or motivate formation of insulative partitions between two separate etching steps, as recited in claim 51.

Further, because Kim does not teach anisotropic etching until Fig. 2A (col. 3, lines 37-44), the cited portions of Kim cannot possibly teach, disclose, suggest or motivate the invention as recited in any of claims 57 and 60-62. For at least these reasons, the rejection of claims 51, 57 and 60-62 based on the teachings of Kim is defective and should be withdrawn, and claims 51, 57 and 60-62 should be allowed.

Summerfelt et al. teach formation of what will later become capacitor dielectric layers 56 using BST (barium strontium titanate) in Figs. 25-28 (see also col. 8, line 36 through col. 9, line 8). A first capacitor electrode is formed atop conductive plug 52, using a platinum layer 74 and a conductive titanium nitride layer 76 (fig. 29; col. 9, lines 8-14). Portions of these conductive layers 74 and 76 formed atop the BST pillars 56 are then removed (Fig. 31; col. 9, lines 16-21).

As a result, an outer electrode comprising platinum 60 and titanium nitride 64 is formed on an outer surface of the capacitor dielectric 56, and an inner electrode comprising platinum 58 and titanium nitride 62 is formed within an inner surface of the capacitor dielectric 56. As noted by Summerfelt et al. (col. 9, lines 26-28), "As can be seen in FIG. 31, the outer electrode can be made common between e.g., all capacitors in a DRAM." As a result, it is apparent that the outer surface of the capacitor dielectric 56 cannot possibly form a second capacitor container, as alleged in the Office Action. For at least these reasons, the rejection of claims 51, 52 and 54-65 over Summerfelt et al. is clearly in error and should be withdrawn, and claims 51, 52 and 54-56 should be allowed.

Claim 57 recites "a method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate."

Summerfelt et al. provide no teaching at all of first and second capacitor container openings. The Office Action is also silent with respect to the invention as recited in claim 57.

Summerfelt et al. teaches anisotropic ion milling of platinum (col. 7, lines 63-65). Summerfelt et al. also teaches anisotropic etching of BST to form capacitor dielectric layer 56 (col. 8, lines 56-60). Summerfelt et al. make no further mention of anisotropic etching. As a result, it is inconceivable that Summerfelt et al. could possibly teach, disclose, suggest or motivate the multiple anisotropic etching steps recited in each of claims 57 and 60-62.

For at least these reasons, the rejection of claims 51, 57 and 60-62 is in error and should be withdrawn, and claims 51, 57 and 60-62 should be allowed.

Dependent claims 52, 54-56, 58, 59 and 63-65 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

For example, claim 55 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings in a first etching step; and anisotropically etching second capacitor container openings in a second etching step", while claim 56 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings", which is not taught, disclosed, suggested or motivated by any of the cited references, and which further appears nowhere in the Office Action.

Additionally, the Examiner's response to argument is deficient in multiple regards. A first deficiency is that the response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §103, or, in the alternative, is an admission that these rejections are defective.

Applicants note the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

A second deficiency is that under the unpatentability rejections, the combinations fail to provide all of the features recited in any of Applicant's independent claims (see MPEP §706.02(j) for criteria for establishing a prima

facie case of unpatentability). The Examiner has ignored these features without providing any appropriate legal basis for doing so.

A third deficiency is the failure to respond to all arguments traversing the unpatentability rejections. Merely repeating that "it would be obvious" to provide the features recited in the claims does not constitute a basis for rejection of the claims. This is particularly true when the references fail to provide the features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

For at least these reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

New claims 66-69 are supported at least by text appearing at p. 6, line 2 through p. 18, line 9 of the specification as originally filed. No new matter is added by new claims 66-69. New claims 66-69 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 51, 52 and 54-69 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The

undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Sept. 26, 2001 By: _____
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/420,635
Priority Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2812
Priority Examiner ..... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO JUNE 26, 2001 FINAL OFFICE ACTION PRELIMINARY AMENDMENT TO ACCOMPANY CPA FILING

Deletions are bracketed, additions are underlined.

In the Specification

The paragraph inserted on p. 1, prior to the Technical Field, by the amendment dated October 21, 1999, has been amended as shown below:

RELATED PATENT DATA

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/036,701, filed March 6, 1998, which is a divisional application of U.S. Patent Application Serial No. 08/742,895, filed November 1, 1996, now U.S. Patent No. 5,998,256.

In the Claims

61. (Amended) A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings in a first dielectric layer;

forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer;

conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave [the] partitions, after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer.

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